

**What is claimed is:**

- 1           1.    A method for fabricating a single-electron transistor  
2   with self-aligned polysilicon sidewall spacer gates on a  
3   silicon-on-insulator (SOI) substrate, comprising the steps of:  
4       depositing a thin oxide layer on a silicon-on-insulator  
5       (SOI) substrate, and performing an ion implantation  
6       to reduce the substrate sheet resistance;  
7       performing electron-beam lithography and etching on the  
8       silicon-on-insulator (SOI) substrate to define  
9       source/drain (S/D) regions and a channel connecting  
10      the source/drain (S/D) regions;  
11      removing the thin oxide layer, and forming an insulating  
12      layer on the substrate;  
13      reducing the width of the insulating layer between about  
14      1 and 40 nm to form a thin wire perpendicularly  
15      intersecting the channel;  
16      forming a gate insulating layer on the substrate; and  
17      forming a plurality of polysilicon sidewall spacer gates  
18      on the sidewalls of the gate insulating layer.
- 1           2.    The method as claimed in claim 1, further comprising  
2   the steps of:  
3       forming a protecting layer on the substrate; and  
4       forming a metal upper gate and Ohmic contact.
- 1           3.    The method as claimed in claim 1, wherein the insulating  
2   layer comprises a silicon dioxide layer and a TEOS layer.

1           4.    The method as claimed in claim 1, wherein the step  
2   of forming a thin wire perpendicularly intersecting the channel  
3   further comprises the step of:

4           electron-beam lithographic etching of the insulating layer  
5           to reduce the width to 80 nm or less; and  
6           further etching of the insulating layer in HF solution to  
7           reduce the width to between about 1 nm and about 40  
8           nm.

1           5.    The method as claimed in claim 3, wherein the silicon  
2   dioxide layer having a thickness of about 50Å and about 500Å  
3   is thermally grown in dry O<sub>2</sub>.

1           6.    The method as claimed in claim 2, wherein the protecting  
2   layer includes a silicon dioxide layer.

1           7.    The method as claimed in claim 1, wherein polysilicon  
2   sidewall spacer gates having a thickness of about 1000Å and about  
3   2000Å is formed by chemical vapor deposition.

1           8.    The method as claimed in claim 1, wherein the  
2   polysilicon sidewall spacer gates having a width of about 10  
3   nm to about 90 nm are formed by dry etching process.

1           9.    A nanoscale single electron transistor, comprising:  
2   a silicon-on-insulator substrate;  
3   a dual polysilicon sidewall spacer gate on the  
4   silicon-on-insulator substrate; the dual polysilicon  
5   sidewall spacer gate separated and symmetric with  
6   an insulating layer;  
7   a source/drain region within the silicon-on-insulator  
8   substrate; and

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9 a channel connecting the source/drain region.

1 10. The single electron transistor of claim 9, wherein  
2 the source/drain region and the channel are formed by  
3 electron-beam lithographic etching.

1 11. The single electron transistor of claim 9, wherein  
2 the width of the dual polysilicon sidewall spacer gate is about  
3 10 nm to about 90 nm.

1 12. The single electron transistor of claim 9, wherein  
2 the insulating layer is perpendicular to the channel.

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